SDR PCB and Schematics Corrections for YU1LM/QRP Projects

Here is list of all my errors in my 3 articles which I knew in this moment. I am so sorry for them and I am apologizing to all for inconveniences. I also want to thank you to all who send me messages about my designs and especially for mistakes which you have found.

1. First part:

-in DR1 78L05 is not oriented correct (turn on it for 180 DEG and shape GND pin)
- In schematic VCC for 74AC02 I missed one choke 100uH, 100uF and 100nF
-better values for R7, R8 are 1K instead 2K2, better ½ VCC divider
-better values for R11, R12in DR2 are 1K instead 2K2, better ½ VCC divider

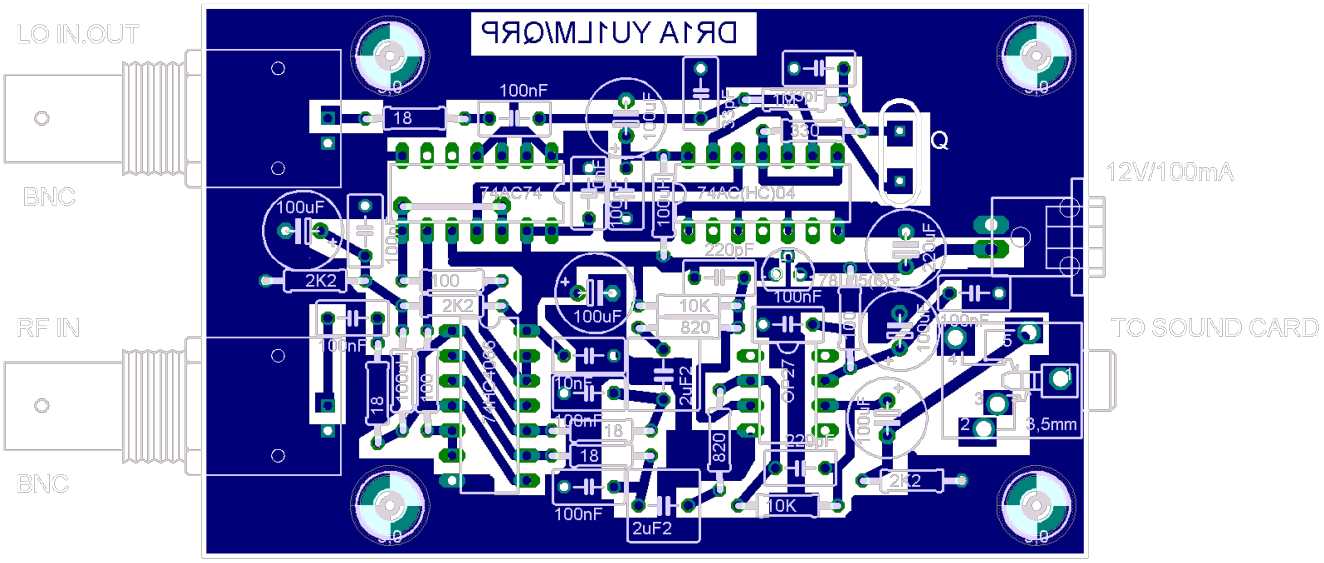
2. Second part:

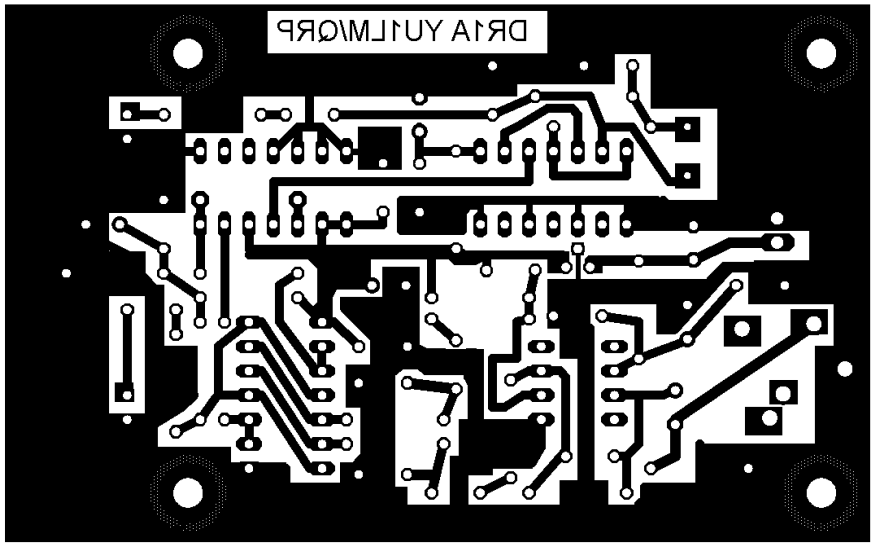
-for IC1 74HC4066 I missed choke 100uH, 100uF and 100nF in +VCC branch

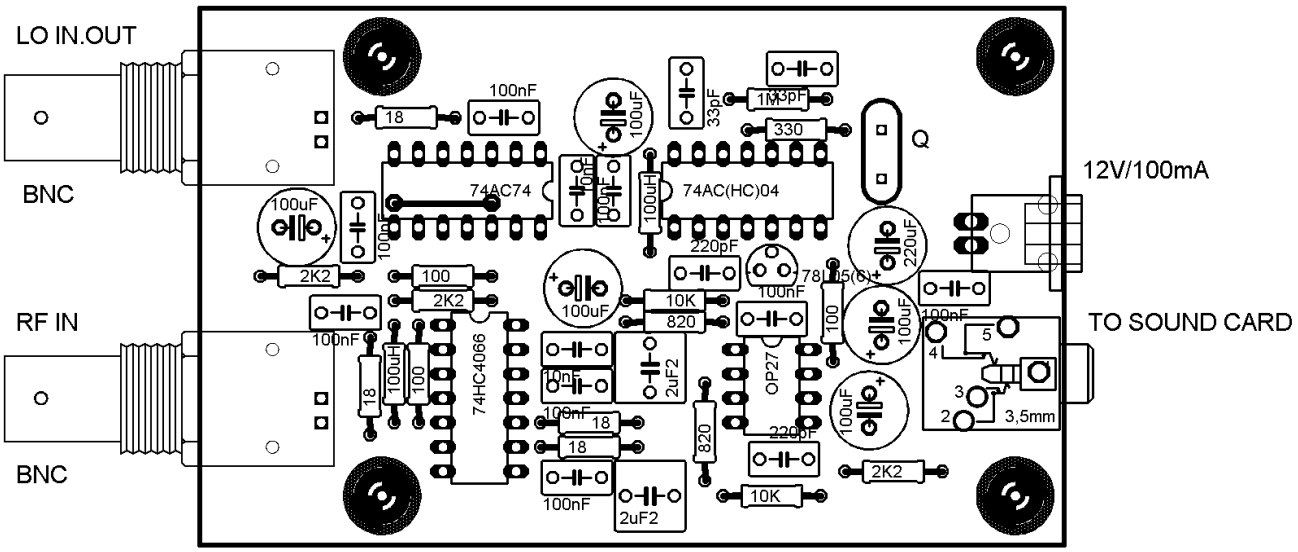
3. Third part:

I made next mistakes:

DR1A correct schematic PCB is down (I turned for 180 DEG 78L05)





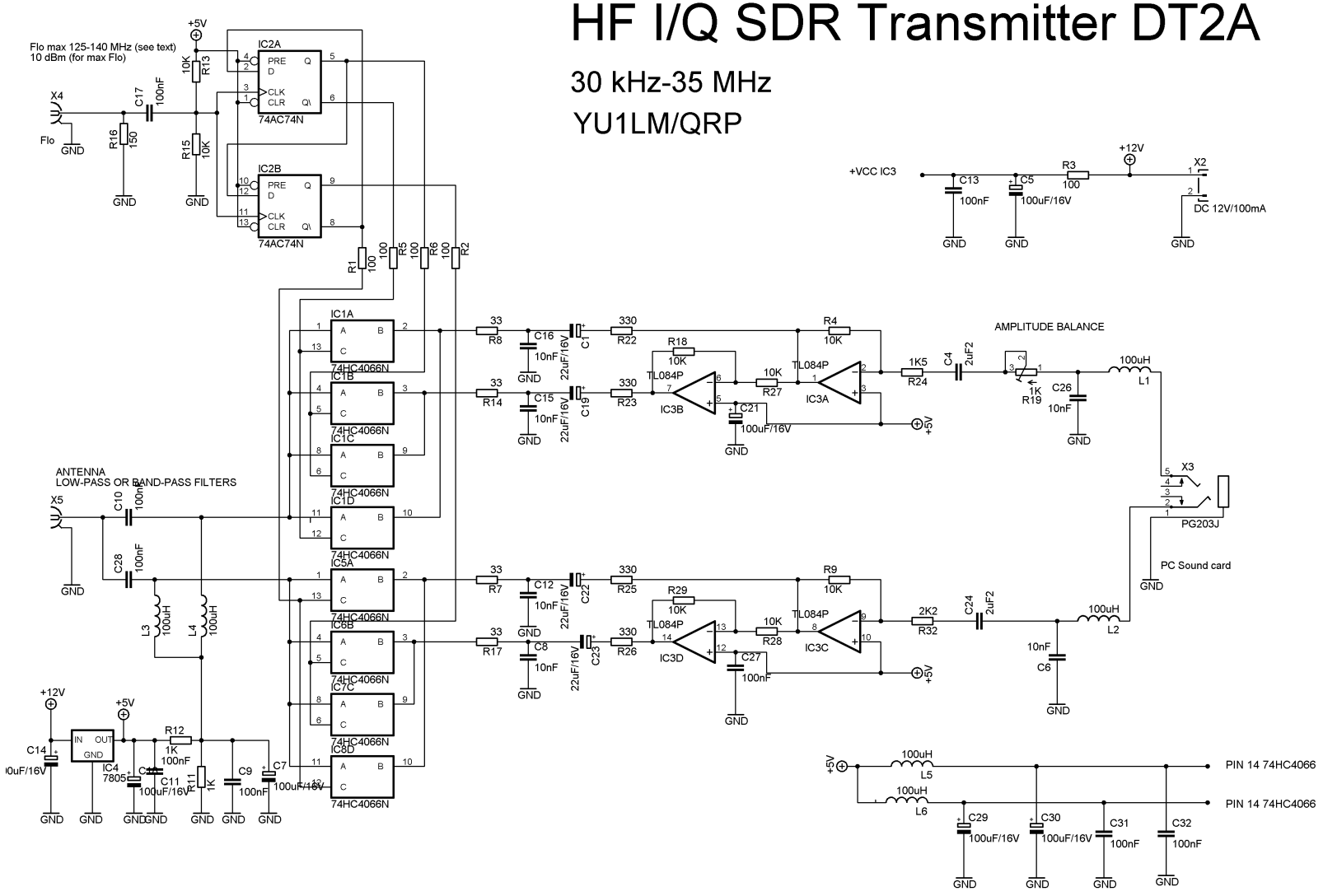


For DT2A SDR Transmitter I published wrong version of schematics. Correct schematic is shown down and PCB published previously was for the DT2A transmitter.

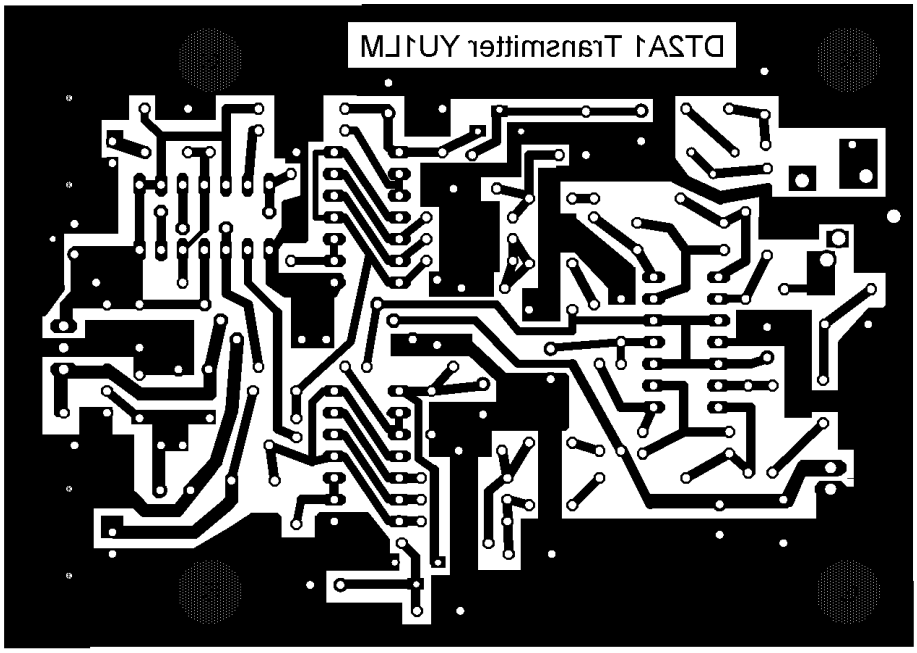
HF I/Q SDR Transmitter DT2A

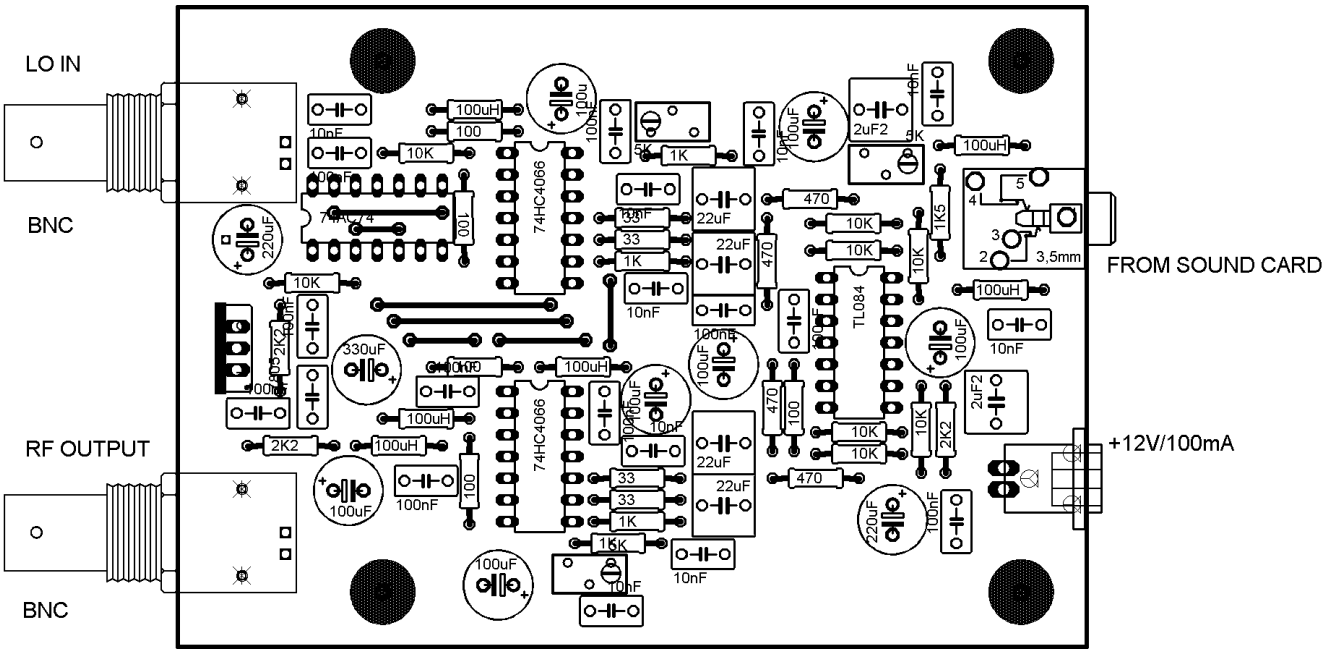
30 kHz-35 MHz

YU1LM/QRP



PCB and parts placement at site article is for this schematic up. DT2A schematic at site is DT2A1 version of DT2A and PCB for it is down with parts placement. I also propose new PCB with lower LO leakage and better LO suppression than original DT2A.

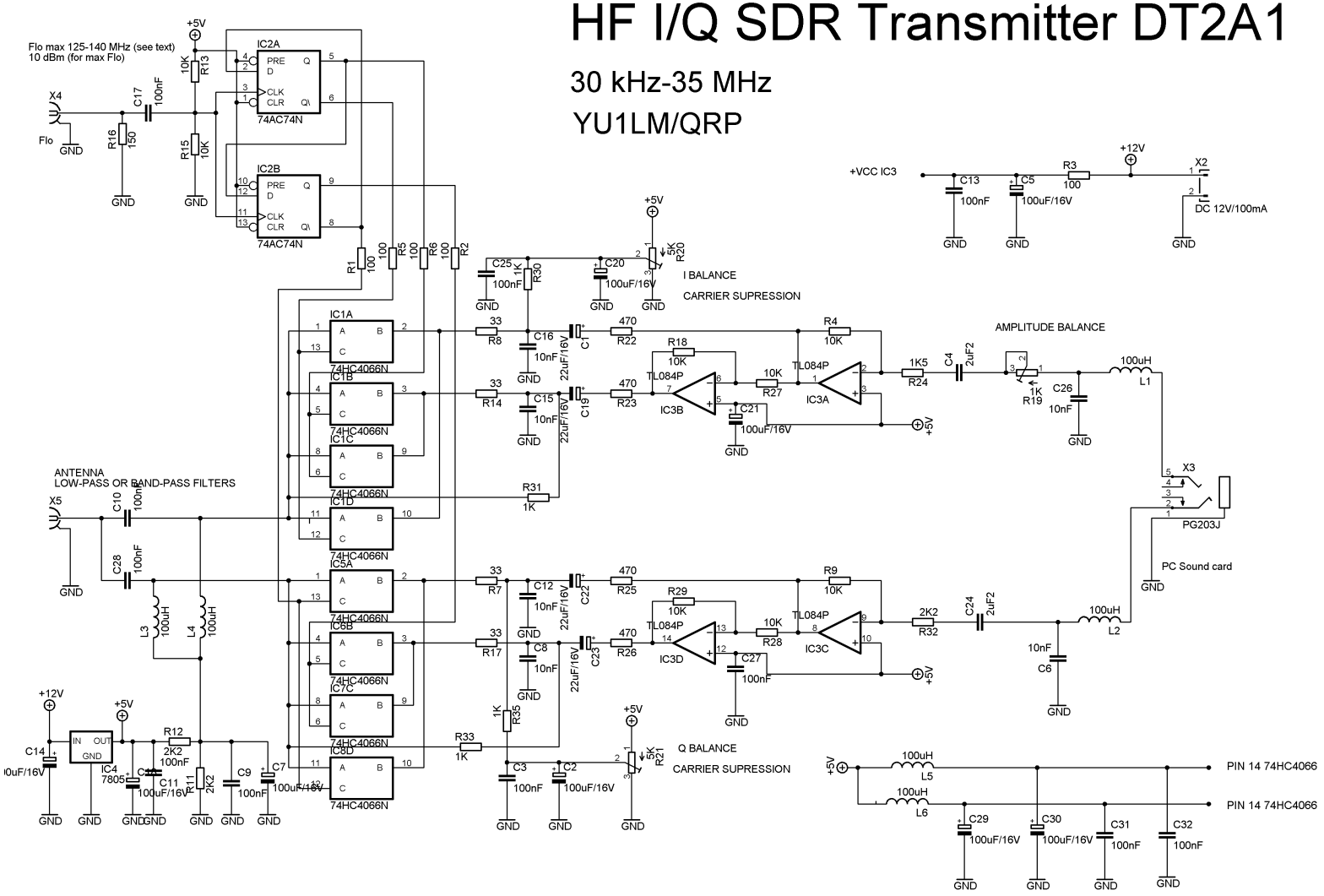




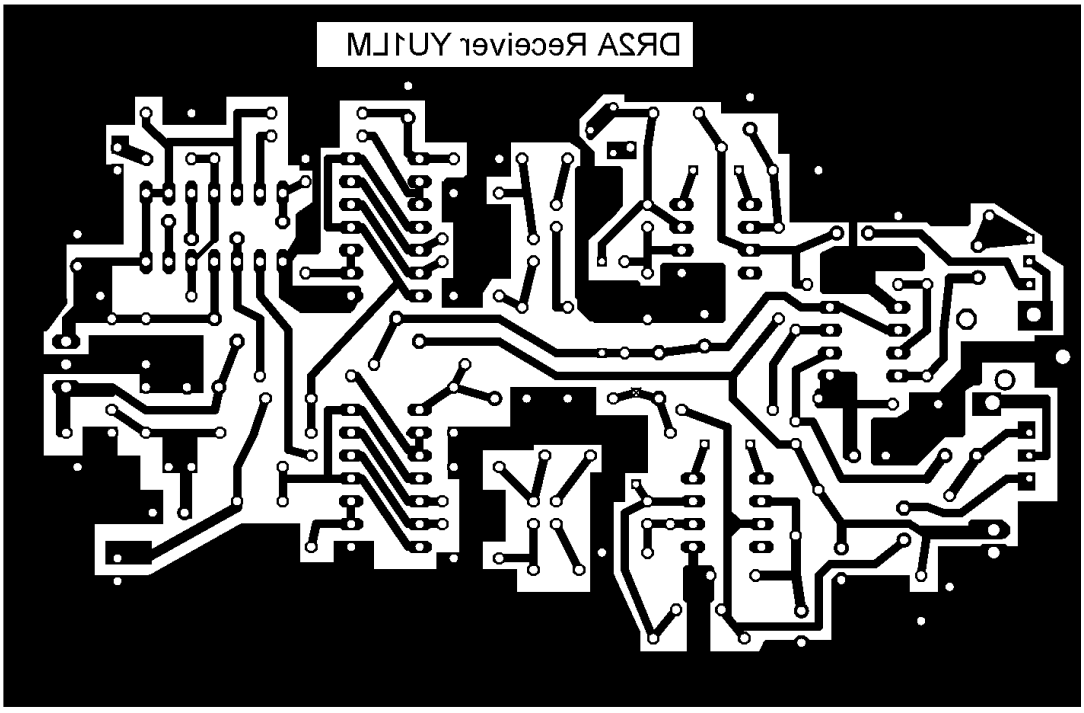
HF I/Q SDR Transmitter DT2A1

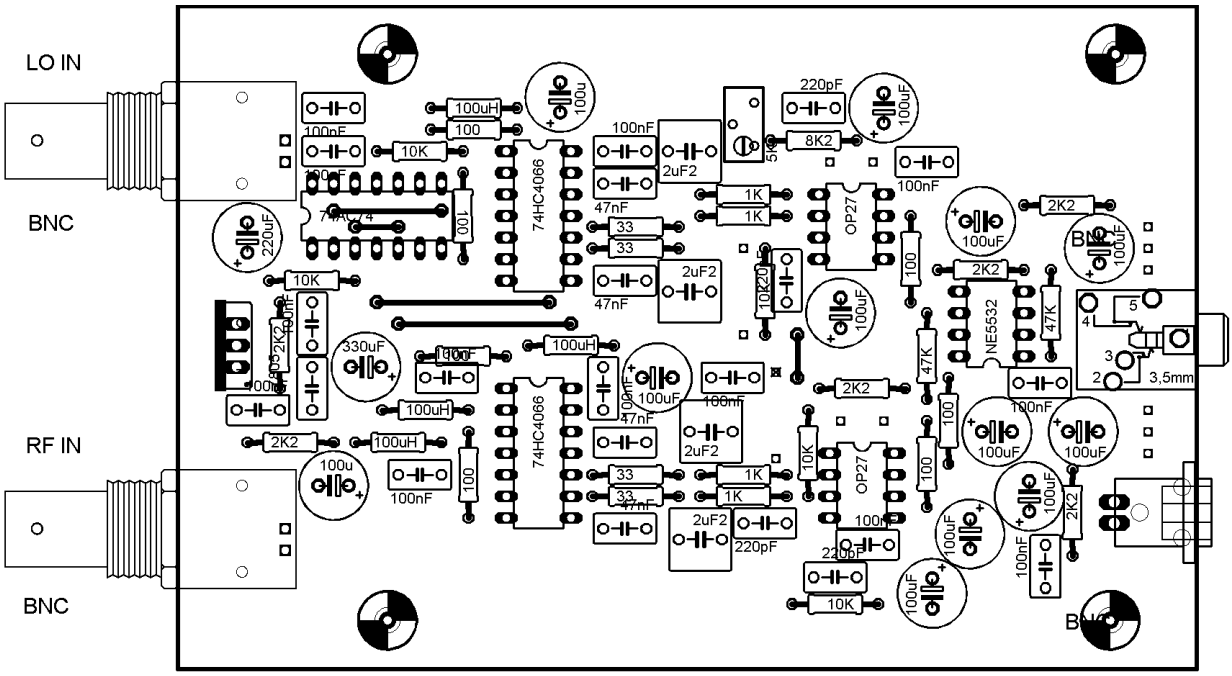
30 kHz-35 MHz

YU1LM/QRP



These corrections are for the third part. DR2A have minor changes and correct schematics PCB and placement for DR2A RX are down.

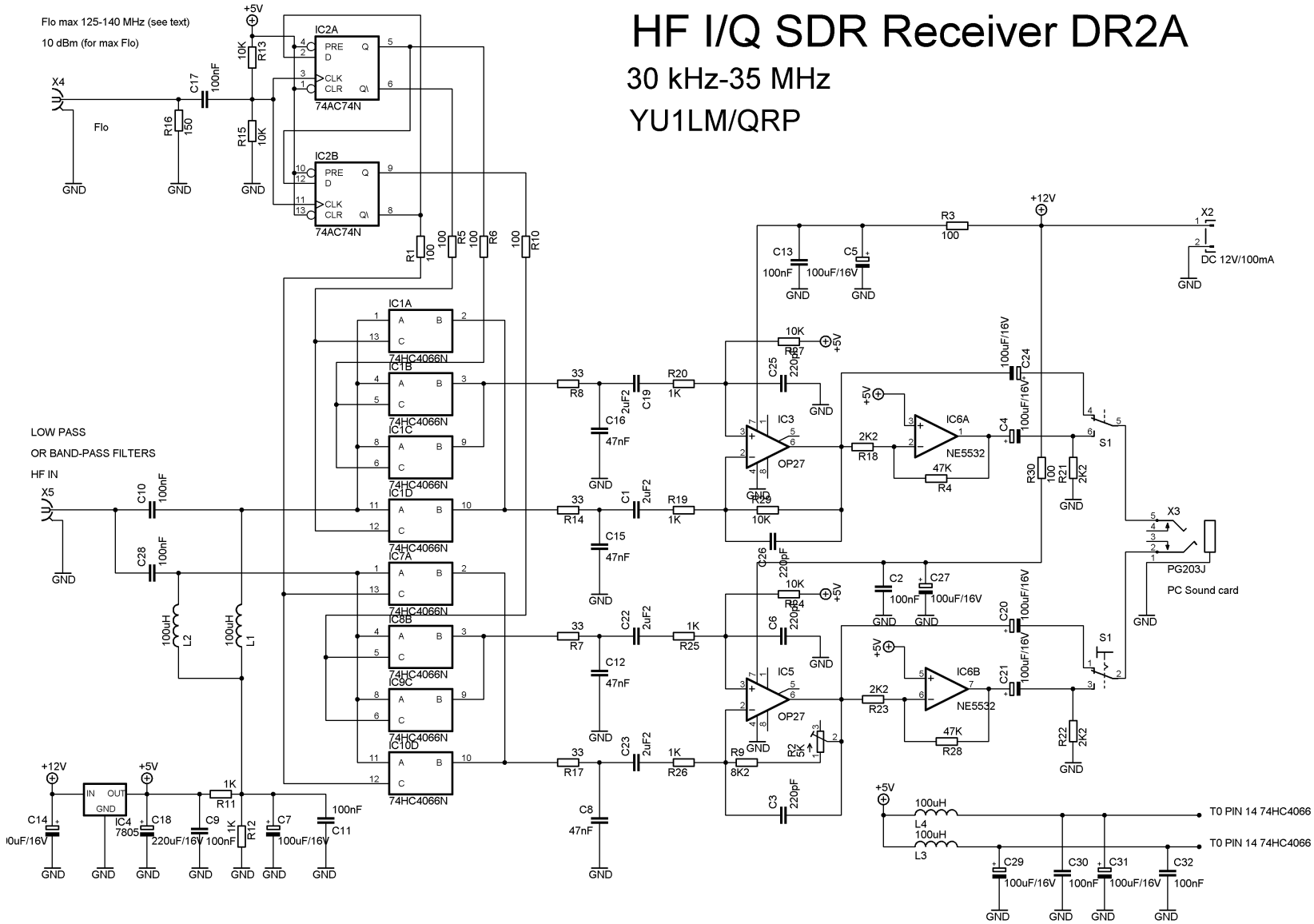




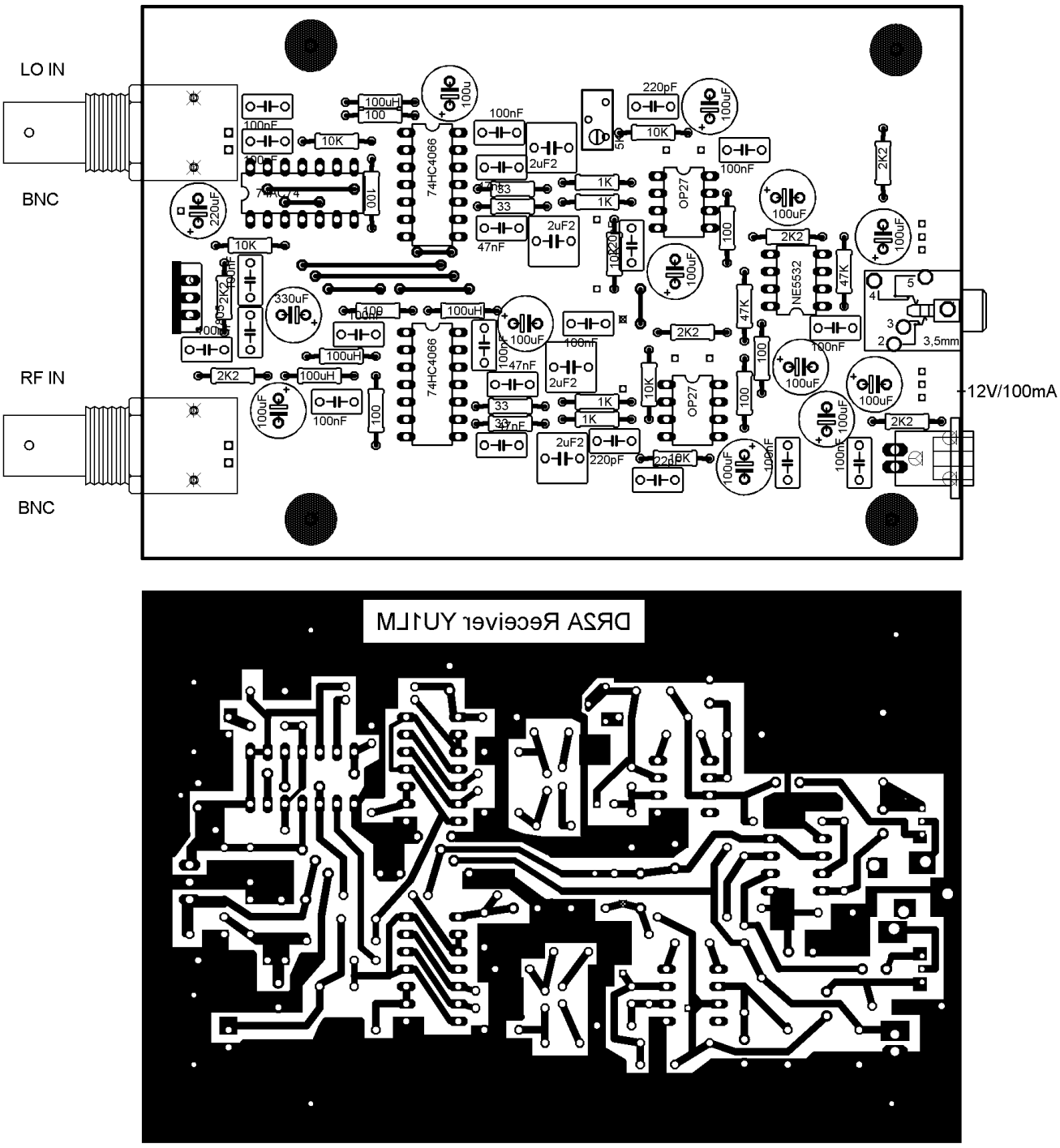
HF I/Q SDR Receiver DR2A

30 kHz-35 MHz

YU1LM/QRP



In meanwhile I made improved PCB for DR2A RX to lower LO leakage see down.



VY 73/72 and GL in SDR homebrew Tasa YU1LM/QRP